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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE						
In re application of: Rene Glaise, et al.	Date: December 8, 2004					
Serial Number: 10/711,320	Examiner:					
Filed: 09/10/2004	Group Art Unit: 2661					
Title: METHOD AND SYSTEM TO ENABLE AN ADAPTIVE LOAD BALANCING IN A PARALLEL PACKET SWITCH	IBM Corporation D/18G, B/300, Zip 482 2070 Route 52 Hopewell Junction, NY 12533-6531					

## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,

Rene Glaise

By:

Joseph P. Abate

Registration No. 30,238

Telephone: (845) 894-4633

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		Proc. ICC'92, 311.1.1-31 HIGH-SPEED ATM NE	Proc. ICC'92, 311.1.1-311.1.5, 1992, by T. ARAMAKI et al., `PARALLEL "ATOM" SWITCH ARCHITECTURE FOR HIGH-SPEED ATM NETWORKS'									
EXAMINER				DATE CONSIDERED								
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